1. (Canceled)

2. (Thrice Amended) A method as recited in Claim 47, wherein said implantation ions comprise ions of said first material and ions that are different from said ions of said first material.

3. (Twice Amended) A method as recited in Claim 2, wherein the implantation ions of said first material comprise silicon ions.

4. (Twice Amended) A method as recited in Claim 3, wherein said first material comprises monocrystalline silicon.

5. (Canceled)

6. (Thrice Amended) A method as recited in Claim 47, further comprising forming spacers in said masking substrate, wherein said unmasked opening is comprised between two adjacent spacers, and each of said spacers extends from the substrate assembly to the top of and in contact with said masking substrate.

7. (Twice Amended) A method as recited in Claim 6, wherein said forming spacers further comprises:

depositing a layer of spacer material over the opening in the masking substrate; and

etching the layer of spacer material to form the spacers around the unmasked opening.

8. (Once Amended) A method as recited in Claim 7, wherein the layer of spacer material comprises silicon nitride.

9. (Thrice Amended) A method as recited in Claim 7, wherein said etching the layer of spacer material is an anisotropic etch.

10. (Thrice Amended) A method as recited in Claim 9, wherein said opening width is in the range from about 0.05 micrometers to about 0.1 micrometers.

11. (Thrice Amended) A method as recited in Claim 47, further comprising the steps, prior to said bombarding through said unmasked opening of:

forming a pad oxide layer on said first semiconductor material;

forming a masking substrate comprising a nitride layer over the pad oxide layer;

forming a photoresist mask over the nitride layer; and

selectively removing the nitride layer through the photoresist mask to expose through said unmasked opening said first semiconductor material, wherein the first semiconductor material is oxidized in the region within said unmasked opening.

12. (Thrice Amended) A method as recited in Claim 11, wherein the photoresist mask is removed after said bombarding through said unmasked opening of said first semiconductor material with implantation ions of said first material.

13. (Once Amended) A method as recited in Claim 11, wherein said selectively removing the nitride layer through the photoresist mask includes selectively removing the nitride layer and selectively removing the pad oxide layer.

14. (Thrice Amended) A method as recited in Claim 47, wherein said semiconductor material has a top surface, and wherein said implantation ions are directed towards said first semiconductor material in a direction that is within ten degrees from a direction that is orthogonal to the top surface.

15. (Thrice Amended) A method as recited in Claim 47, wherein said forming an oxide further comprises heating said substrate assembly while exposing the substrate assembly to oxygen.

16. (Thrice Amended) A method as recited in Claim 47, wherein said first semiconductor material comprises a monocrystalline material having a lattice structure, wherein the implantation ions cause the lattice structure of the monocrystalline material to become partially randomized at the region into which said ions are implanted.

17. (Twice Amended) A method as recited in Claim 16, wherein both the monocrystalline material and said implantation ions comprise silicon.

18. (Thrice Amended) A method as recited in Claim 47, wherein said exposing said implanted region is conducted at a pressure in the range from about 1 atmosphere to about 25 atmospheres.

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19. (Thrice Amended) A method as recited in Claim 47, wherein said exposing said implanted region is conducted at a pressure in the range from about 5 atmospheres to about 25 atmospheres.

20. (Thrice Amended) A method for forming an oxide region on a substrate assembly, the method comprising the steps of:

forming a hard mask over a volume of silicon of a substrate assembly;

forming an opening in the hard mask to expose a region of the volume of silicon;

bombarding the exposed region of the volume of silicon with silicon ions through the opening in the hard mask so as to leave unaltered the conductivity type of the exposed region of the volume of silicon; and

oxidizing the volume of silicon by exposure through said opening to oxygen of an exposed surface thereof to form silicon dioxide substantially only at the region exposed to oxygen, wherein said silicon dioxide has substantially uniform thickness throughout said region, wherein said bombarding and said oxidizing are performed through said opening having a width that is substantially the same at said bombarding as it is at said oxidizing, and wherein no additional layer is formed within said opening after said bombarding and prior to said oxidizing.

21. (Thrice Amended) A method as recited in Claim 20, further comprising forming a spacer around the opening in the hard mask, said spacer extending from the volume of silicon to contact the hard mask, wherein said bombarding the exposed region of the volume of silicon with silicon ions through the opening in the hard mask implants ions immediately adjacent to but not through the spacer around the opening in the hard mask, and wherein said oxidizing and said bombarding are performed through the same opening.

22. (Twice Amended) A method as recited in Claim 21, wherein said forming a spacer around the opening in the hard mask comprises:

depositing a layer of spacer material over the opening in the hard mask; and

anisotropically etching the layer of spacer material at the opening in the hard mask to form the spacer situated around the opening of the hard mask.

23. (Once Amended) A method as recited in Claim 21, wherein the spacer around the opening in the hard mask comprises silicon nitride.

24. (Twice Amended) A method as recited in Claim 21, wherein the spacer is one of a pair of spacers, the ions being implanted in between but not through the pair of spacers and past the hard mask into the exposed region of the volume of silicon, and wherein the exposed region is situated between the pair of spacers, whereby the silicon dioxide is not substantially formed underneath the pair of spacers.

25. (Twice Amended) A method as recited in Claim 24, wherein the pair of spacers are separated by a distance in the range of about 0.05 micrometers to about 0.1 micrometers.

26. (Twice Amended) A method as recited in Claim 20, further comprising forming a pad oxide layer upon the volume of silicon prior to forming a hard mask over a volume of silicon of a substrate assembly, the hard mask being formed upon the pad oxide layer, and said forming a hard mask over a volume of silicon of a substrate assembly comprising:

forming the hard mask upon the pad oxide layer; and

forming a photoresist mask over the hard mask; and wherein silicon dioxide is formed in the volume of silicon at the region beneath the opening in the hard mask.

27. (Twice Amended) A method as recited in Claim 26, wherein the photoresist mask is removed after said bombarding the exposed region of the volume of silicon.

28. (Once Amended) A method as recited in Claim 26, wherein said etching the hard mask also etches through the pad oxide layer.

29. (Twice Amended) A method as recited in Claim 20, wherein the exposed region of a volume of silicon has a top surface, and said bombarding the exposed region of the volume of silicon with silicon ions through the opening in the hard mask is conducted such that the direction that the ions are implanted into the exposed region is within ten degrees from a direction that is orthogonal to the top surface.

30. (Twice Amended) A method as recited in Claim 20, wherein said oxidizing the volume of silicon to form silicon dioxide substantially only at the exposed region by exposure of the exposed region to oxygen further comprises heating the substrate assembly while exposing the substrate assembly to oxygen.

31. (Twice Amended) A method as recited in Claim 20, wherein the volume of silicon comprises monocrystalline silicon having a lattice structure, and wherein the implanted silicon ions

in the monocrystalline silicon cause the lattice structure of the monocrystalline silicon to become partially randomized at the exposed region into which the ions are implanted.

32. (Thrice Amended) A method for forming an oxide region on a substrate assembly, the method comprising the steps of:

forming a hard mask over a pad oxide layer situated on a volume of silicon of a substrate assembly, the substrate assembly having a top surface;

forming an opening in the hard mask to expose a region of the volume of silicon, said region of said volume of silicon comprising monocrystalline silicon having a lattice structure;

depositing a layer of silicon nitride over the opening of the hard mask;

etching the layer of silicon nitride and the pad oxide layer to form a pair of silicon nitride spacers situated on opposite sides of the opening of the hard mask and having said exposed region of the volume of silicon therebetween, each said silicon nitride spacer extending from the volume of silicon to contact the hard mask; and

forming silicon dioxide in the region between said pair of spacers by kinetically regulating silicon oxidation, wherein said kinetically regulating silicon oxidation comprises:

implanting silicon ions between but not through the pair of silicon nitride spacers and through the opening in the hard mask into the exposed region of the volume of silicon such that the direction that the silicon ions are implanted into the exposed region is within ten degrees of a direction that is orthogonal to the top surface of the substrate assembly, wherein the implanted silicon ions do not substantially alter the conductivity type of the region, and wherein the implanted silicon ions in the monocrystalline silicon in the exposed region cause the lattice structure thereof to become partially randomized; and

heating the substrate assembly and exposing the substrate assembly t o

oxygen so as to form silicon dioxide at the exposed region, whereby the silicon layer oxidizes faster where the silicon ions are implanted than where the silicon ions are not implanted, wherein said silicon dioxide has substantially uniform thickness throughout said exposed region, wherein said kinetically regulating silicon oxidation is performed through said opening having a width that is substantially the same at said implanting as it is at said heating and said exposing, and wherein no additional layer is formed within said opening during said kinetically regulating silicon oxidation.

33. (Twice Amended) A method as recited in Claim 32, wherein the pair of spacers are separated by a distance in the range of about 0.05 micrometers to about 0.1 micrometers.

45. (Once Amended) A method as recited in Claim 47, wherein said implantation ions are different from ions of said first semiconductor material.

46. (Once Amended) A method as recited in Claim 47, further comprising bombarding through said unmasked region with implantation ions that are different from ions of said first semiconductor material.

47. (New) A method for forming an oxide region on a substrate assembly, the method comprising:

providing a substrate assembly having a first semiconductor material and a masking substrate thereover, wherein said masking substrate comprises an unmasked opening that has an opening width, such that said unmasked opening is defined by a masking substrate-free region on said substrate assembly, wherein said masking substrate-free region has a width that is said opening width;

selecting ions to be implanted into said first semiconductor material as implantation ions, wherein said selecting is performed such that said ions do not alter the electrical charge characteristics of said first semiconductor material, and such that said masking substrate is impermeable to said ions;

bombarding through said unmasked opening said first semiconductor material with implantation ions to produce an implanted region; and

forming an oxide of said first semiconductor material of substantially uniform thickness throughout said opening width by exposing said implanted region to a gas phase oxidant, wherein said bombarding and said exposing are performed through said unmasked opening, and said bombarding and said exposing are performed over the entire opening width of said unmasked opening, and no additional layer is formed within said unmasked opening after said bombarding and prior to said forming an oxide.

48. (New) A method as recited in Claim 1, wherein said implantation ions are ions of said first semiconductor material.